In the Claims:

Please cancel claims 1-10 and add the following new claims:

1-10. (Cancelled)

11. (New) An information processing unit,

adding instruction codes which are different from each other in the same group of instruction to each instruction, and sorting the instructions executable into a plurality of groups of instructions,

comprising a decoder circuit selecting the group of instruction corresponding to the instruction code inputted thereto, based on input history of the instruction code, to determine the instruction to be executed uniquely by the instruction code inputted thereto, and

setting a prescribed instruction code, which assigns an optional instruction depending on the other group of instruction, to each group of instructions, and wherein said decoder circuit controls to execute the instruction which is assigned to said prescribed instruction code, when said prescribed instruction code is inputted.

12. (New) The information processing unit according to claim 11, wherein said instruction depending on the other group of instruction, which is assigned to said prescribed instruction code, can be changed.

13. (New) The information processing unit according to claim 11, wherein a plurality of said prescribed instruction codes, which assign optional instructions depending on the other group of instruction, are provided to groups of the instruction.

14. (New) An information processing unit,

adding instruction codes which are different from each other in the same group of instruction to each instruction, and sorting the instructions executable into a plurality of groups of instructions, and

comprising a decoder circuit holding a prescribed information corresponding to input history of the instruction codes, selecting the group of the instruction corresponding to the instruction code inputted thereto, based on said prescribed information, to determine the instruction to be executed uniquely by the instruction code inputted thereto,

wherein said decoder circuit changes said prescribed information temporary, when a prescribed instruction code is inputted.

15. (New) The information processing unit according to claim 14, wherein said decoder circuit determines the instruction to be executed, regardless of said prescribed information corresponding to the input history of the instruction codes, when an instruction code for determining the instruction to be executed uniquely by only the instruction code inputted thereto is inputted.

16. (New) An information processing unit executing an instruction which is determined by an instruction code inputted thereto,

comprising a decoder circuit holding a prescribed information corresponding to input history of a plurality of instruction codes inputted thereto, determining the instruction to be executed uniquely, based on the instruction code inputted thereto as well as the prescribed information, from a plurality of instructions which are assigned to the said instruction code inputted thereto.

17. (New) The information processing unit according to claim 16, wherein the instructions executable are sorted into a plurality of groups of instructions and the instruction codes which are different from each other in the same group are added to each instruction.

18. (New) The information processing unit according to claim 16, wherein said decoder circuit determines the instruction to be executed, regardless of said

prescribed information corresponding to the input history of the instruction codes, when an instruction code for determining the instruction to be executed uniquely by only the instruction code inputted thereto is inputted.

19. (New) An information processing unit, comprising a plurality of processors which execute instructions independently in one chip, wherein the instructions executable by said processor are sorted into a plurality of groups of instructions indicated by a group code, with the instruction codes which are different from each other in the same group of instruction being added to each instruction, and wherein said each processor comprises a decoder circuit which determines the instruction to be executed uniquely based on said group code corresponding to input history of the instruction codes and the instruction code inputted thereto, and a processor element which executes an operation corresponding to a control signal supplied from said decoder circuit, and wherein the instruction executable by said processor includes an alias instruction which assigns in advance the optional instruction for the internal instruction code generated by the group code and the input instruction code.

20. (New) The information processing unit according to claim 19, wherein said each processor further comprises a group resister which stores the group codes set on the basis of the input history of said instruction code.

21. (New) The information processing unit according to claim 20, wherein said each processor further comprises a look up table which defines the rule for changing the group code stored in said group register.

22. The information processing unit according to claim 21, wherein said look up table defines a combination of an instruction mask for setting bit to be masked, an instruction code for comparing the instruction with the internal instruction code generated by the group code and the input instruction code, and a changed group code.